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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/080,576	02/25/2002	Hirofumi Shibuya	XA-9628	8735

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EXAMINER	
HO, THANG H	

ART UNIT	PAPER NUMBER
2188	7

DATE MAILED: 12/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/080,576	SHIBUYA ET AL.	
	Examiner	Art Unit	
	Thang H Ho	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy filed on 04/26/2002 has been received.

Information Disclosure Statement

2. The information disclosure statement (IDS) filed on 02/25/2002 has been received and considered. Please see attached PTO-1449.

3. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

Specification

4. Claims 1-21 are presented for examination.

5. The disclosure is objected to because of the following informalities:

On page 3, the recitation of "flush EEPROM" should be changed to read --flash EEPROM--.

On page 14, the recitation of "host device 2" should be changed to read --host device 20--.

On page 18, the recitation of "can be cahnged" should be changed to read –can be changed--.

Appropriate correction is required.

6. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is required in correcting any errors of which applicant may become aware in the specification. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

8. Claims 1-3, 11-13 and 17-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirabayashi et al. (United States Patent 6,219,768), hereinafter Hirabayashi.

As per claim 1, Hirabayashi discloses in figure 2 a memory unit (20) including a memory device (21) having at least a data unit and a management unit corresponding to the data unit [column 2, lines 19-22 *""...storage means for storing data and the area management information...*"], wherein said memory device is divided into a plurality of memory areas [(FIG. 3A, reference "BLOCK")], management information capable of

controlling separately each of the memory areas for accessing from outside is tabled in the data unit, and control information for setting a limit to accessing a prescribed memory area of the plural memory areas is included in the management information [(see figures 3A-3C and column 7, lines 10-49 *"...Each block... is made up of plural pages... data are read out by the controller 25... Each page... has a data storage area and a management information storage area... "*)].

As per claim 2, Hirabayashi discloses in figure 2 a memory unit (20) including a memory device (21) having at least a data unit and a management unit corresponding to the data unit [column 2, lines 19-22 *""...storage means for storing data and the area management information..."*], wherein the memory device is divided into a plurality of memory areas [(FIG. 3A, reference "BLOCK")], management information capable of controlling separately each of the memory areas for accessing from outside is tabled in the data unit, wherein the management information includes a first control information prohibiting writing data in a prescribed memory area of the plural memory areas [(column 9, lines 25-28 *"The management flag specifies bock attributes... specifies... the block being a read-only..."*)], a second control information prohibiting reading out data from a prescribed memory area of the plural memory areas [(column 9, lines 25-28 *"The management flag specifies bock attributes... specifies... the block... being also writeable."*)] and a third control information storing data that are written in a prescribed memory area of said plural memory areas in plural places nearly at a same time [(FIG. 3C, reference SPARE DISTRIBUTED MANAGEMENT INFORMATION and column

7, lines 62-67 *"There is also stored, as the spare distributed management information, the same management information as the distributed management information..."*)].

As per claim 3, Hirabayashi discloses the memory unit (20) wherein the management information includes control information for identifying whether or not a memory area which is kept as a spare area in advance is capable of being used [(FIG. 3C, reference "SPARE DISTRIBUTED MANAGEMENT INFORMATION" and column 7, lines 62-67 *"There is also stored, as the spare distributed management information, the same management information as the distributed management information..."*)].

As per claim 11 and 17-21, Hirabayashi discloses in FIG. 2 a data processing system (1), wherein a memory unit (21) and a host device (10) capable of accessing it are included and the host device (10) includes an information processing unit for controlling separately the memory area based on the management information [(column 5, lines 22 through column 7, lines 7)].

As per claim 12, Hirabayashi discloses a method for controlling a memory device including at least one semiconductor memory chip having a data unit and a management unit corresponding to said data unit [column 2, lines 19-22 *""...storage means for storing data and the area management information..."*], wherein, when said memory device is divided into plural memory areas [(FIG. 3A, reference BLOCK)], the method comprises a step for controlling separately the memory device by each memory area based on

management information that is tabled on said data unit, by including a first control information prohibiting writing data in a prescribed memory area of the plural memory areas [(column 9, lines 25-28 *"The management flag specifies bock attributes... specifies... the block being a read-only..."*)], a second control information prohibiting reading out data from a prescribed memory area of the plural memory areas [(column 9, lines 25-28 *"The management flag specifies bock attributes... specifies... the block.... being also writeable."*)] and a third control information storing data that are written in a prescribed memory area of said plural memory areas in plural places nearly at a same time [(FIG. 3C, reference "SPARE DISTRIBUTED MANAGEMENT INFORMATION" and column 7, lines 62-67 *"There is also stored, as the spare distributed management information, the same management information as the distributed management information..."*)].

As per claim 13, Hirabayashi further discloses that the method for controlling a memory device according to claim 12, wherein said management information includes a control information for identifying whether or not a memory area is usable [(FIG. 3C, reference "POSSIBLE/NOT POSSIBLE FLAG" and column 8, lines 49-50 *"The possible/not possible flag denotes whether a block is in the usable sate or in the non-usable state."*)].

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 4-7, 9-10 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirabayashi et al. (United States Patent 6,219,768), hereinafter Hirabayashi, in view of Ma et al. (United States Patent 5,956,473), hereinafter MA.

As per claims 4 and 14, Hirabayashi discloses the memory unit substantially as claimed.

However, Hirabayashi fail to disclose the management information comprising control information for indicating erasing number of times or rewriting number of times of a memory area.

Ma teaches the usage of a wear leveling method comprising control information for indicating erasing number of times or rewriting number of times of a memory area [(Abstract *"The present application also discloses a war leveling method in which the difference between the number of erasures of any two blocks ... "*, column 8, lines 33-65 *"... the attribute "age count" is increased by 1 every time a block is erased..."*)].

Accordingly, it would have been prima facie obvious for one skilled in the art at the time the invention was made to implement the system and method as taught by Hirabayashi and utilize a wear leveling method as taught by Ma to generate the claimed invention with a reasonable expectation of success.

One skilled in the art would have been motivated to do so, because it would equalize the amount of erasure for all the bocks within the memory unit reducing the chance that any one block of the memory unit from premature failing, thereby extending the life of the memory unit as pointed out by Ma starting on column 10, lines 60 through column 11, lines 11. .

As per claim 5, Hirabayashi discloses in FIG. 2 that a memory means (21) for storing the management information altogether (i.e. within the memory blocks) is included [(see FIGS. 3A-3C)].

As per claim 6, Hirabayashi discloses that an area for storing the management information by each memory area is provided in the plural memory areas [(see FIGS. 3A-3C)].

As per claim 7, Hirabayashi discloses that the control means for controlling separately the memory area based on the management information is included [(FIG. 2, references 25-26)].

As per claim 9, Hirabayashi discloses that the control means includes a controlling unit for processing [(FIG. 2, reference 26)] the management information by exclusive hardware [(column 6, lines 5 –56)].

As per claim 10, Hirabayashi discloses that a memory unit and a host device capable of accessing it are included [(FIG. 2, references 10 and 20)].

As per claim 15, Hirabayashi discloses that the method includes a first step having a management information edit step capable of editing the management information and identifying whether or not the step of editing the management information transits to an edit mode of the management information and a second step for editing the management information in an edit mode which is transited based on an identifying result at the first step [(FIG. 2, column 6, lines 31-41 *"... The controller **26** causes the area management flag... to be written in the flash memory **21**."*)].

11. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirabayashi et al. (United States Patent 6,219,768), hereinafter Hirabayashi, in view of Ma et al. (United States Patent 5,956,473), hereinafter MA, as applied to claims 4-7, 9-10 and 14-16 above, and further in view of Ritchie (United States Patent 4,135,240).

As per claim 8, the combination of Hirabayashi and Ma memory unit discloses the invention substantially as claimed including the control means comprising a controlling unit for processing [(FIG. 2, reference 26)] the management information by exclusive hardware [(column 6, lines 5 –56)].

However neither Hirabayashi nor Ma discloses expressly the control means includes a micro processing unit (inherent) for processing the management information by software.

Ritchie teaches an improved arrangement for controlling access to data files in the memory, the access control can be expressed either in terms of a computer program (software) or a computer circuitry (hardware), wherein the two being functional equivalents of one another, so that to have a flexible way of access control, since for some purposes a software may be preferable and for others hardware may be preferable [(Ritchie, column 5, lines 42-60)].

Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the current invention was made to employ Ritchie's teaching into the combination of Hirabayashi and Ma memory unit in order to have design flexibility for access control since for some purposes a software may be preferable and for others hardware may be preferable.

Allowable Subject Matter

12. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Form PTO-892.

14. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to (703) 872-9306

Hand–delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA. Sixth Floor (Receptionist).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thang H Ho whose telephone number is 703-305-1888. The examiner can normally be reached on Monday-Friday from 7:00 A.M. - 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Thang Ho
Art Unit 2188
November 25, 2003

Kevin L. Ellis
Primary Examiner